

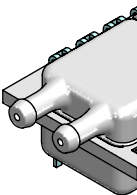
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NOTES: UNLESS OTHERWISE SPECIFIED

1. INPUT
OPERATING SUPPLY VOLTAGE RANGE (Vs): 2.7 TO 5.5 VDC
INPUT VOLTAGE PROTECTION: -0.3 TO 6 VDC ON Vin PIN,
-0.3 TO Vs+0.3 ON ALL OTHER PINS
PROOF PRESSURE (MIN): 1.0 PSI (70 mbar)
BURST PRESSURE (MIN): 1.5 PSI (103.4 mbar)

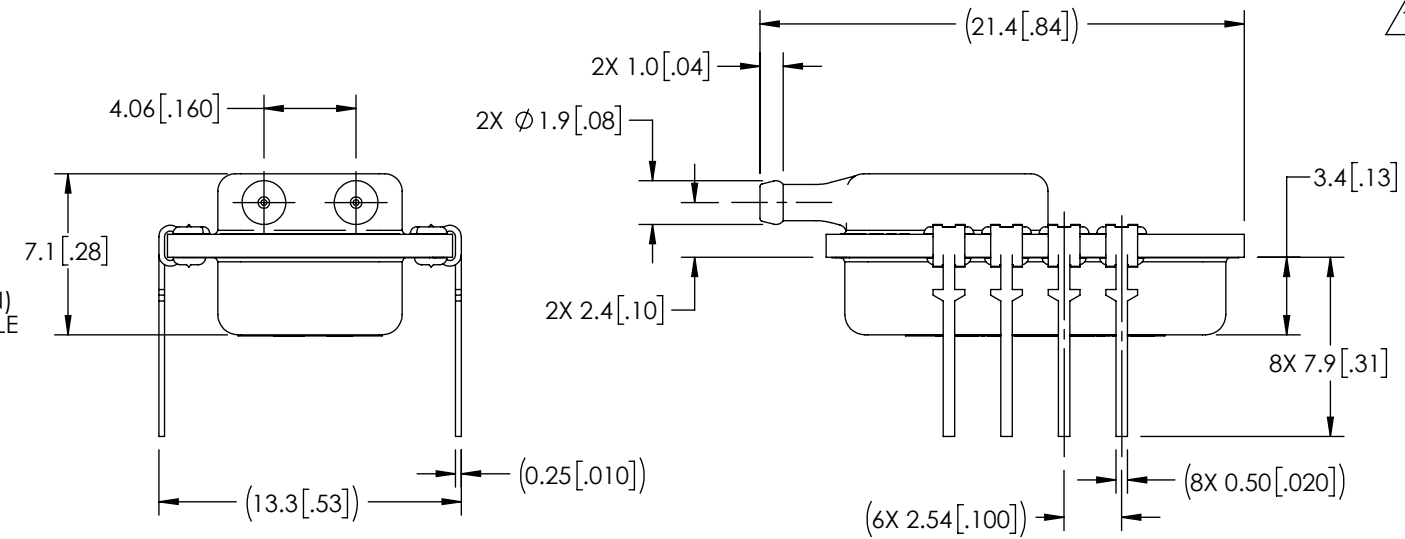
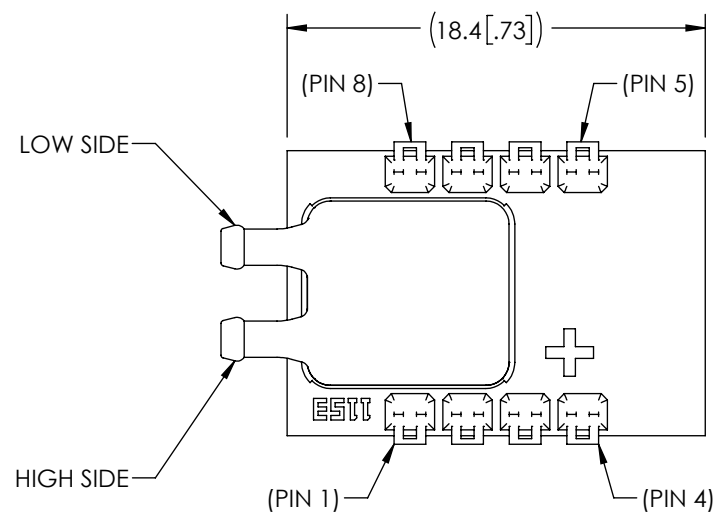
2. OUTPUT:
14-BIT DIGITAL OUTPUT COUNT
DIGITAL COUNT AT NULL (0% FS): 1638
DIGITAL COUNT AT FULL SCALE (100% FS): 14745

RANGE	TOTAL ERROR BAND AT 25°C
0-2" 0-5mbar	2% OF SPAN
±2" ±5mbar	1% OF SPAN
0-5" 0-12.5mbar	
±5" ±12.5mbar	
0-10" 0-25mbar	

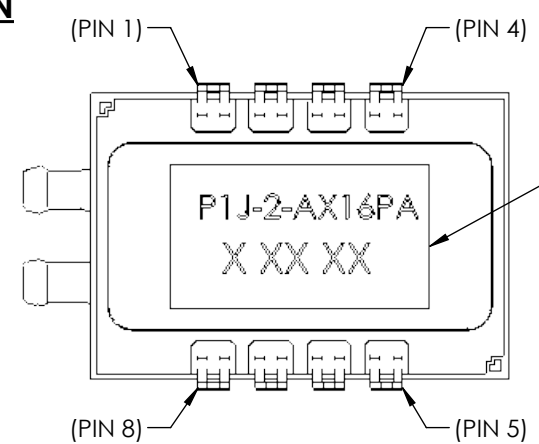
3. TEMPERATURE ERROR (0 TO 60°C): 0.05% / °C (% OF FULL SCALE SPAN)
TEMPERATURE ERROR (-20 TO 0°C AND 60 TO 85°C): 5% OF FULL SCALE SPAN
 4. ACCURACY: 0.25% MAX (% OF FULL SCALE SPAN)
(RSS OF LINEARITY, HYSTERESIS AND REPEATABILITY)
 5. EXCITATION CURRENT: < 2.5mA
 6. RESPONSE TIME: 0.5 ms
 7. ENVIRONMENTAL
OPERATING TEMPERATURE RANGE: -20°C TO 85°C
STORAGE TEMPERATURE RANGE: -40°C TO 85°C
VIBRATION: 10 G'S PEAK TO PEAK SINUSOIDAL (20 TO 1600Hz)
SHOCK: 50 G'S, 1/2 SINEWAVE, 11mSEC PULSE, 18 PULSES (6 PER AXIS)
 8. HUMIDITY: UP TO 92% RH IN A NON-CONDENSING ENVIRONMENT
 9. RELIABILITY:
EXPECTED OPERATING LIFE: 10 MILLION FULL PRESSURE CYCLES MINIMUM
SHELF LIFE: 10 YEARS MINIMUM
STABILITY: ±1% OF FULL SCALE SPAN FOR 1 YEAR
 10. MATERIAL:
SUBSTRATE: ALUMINA
COVERS: PPS, 40% GLASS FILLED, BLACK
SEAL: SILICONE
TERMINAL PINS: PHOSPHOR BRONZE, TIN PLATED
 11. MEDIA: DRY AIR
 12. PRESSURE CONNECTIONS: TUBE FITTING
 13. WEIGHT: 3.5g MAX
 14. ORIENTATION SENSITIVITY:
± 0.1% OF FULL SCALE SPAN
- 

15. CALIBRATION SOFTWARE FOR SPI OUTPUT HAS NOT BEEN IMPLEMENTED, PLEASE CONTACT THE FACTORY FOR FUTURE REQUEST.

	OUTPUT TYPE	
PIN #	-8 (SPI)	-A THRU -F (I ² C)
1	GND	GND
2	VSUP	VSUP
3	MISO	SDA
4	SCLK	SCL
5	SS	INT
6	N/C	N/C
7	N/C	N/C
8	N/C	N/C



P1J-2-AX16PA SHOWN



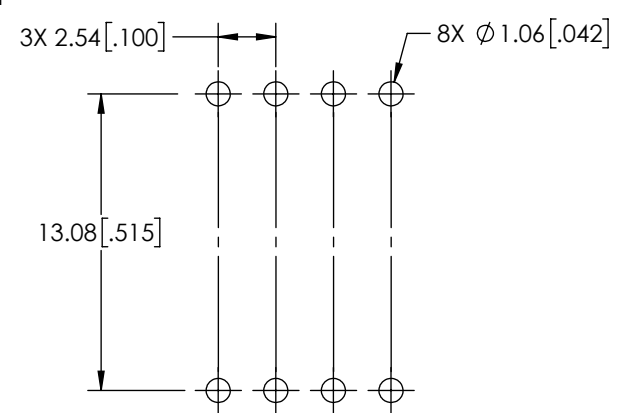
— LABEL
KAVLICO PN
DATE CODE

DATE CODE EXAMPLE: C 1 0 1 5

C MARCH _____

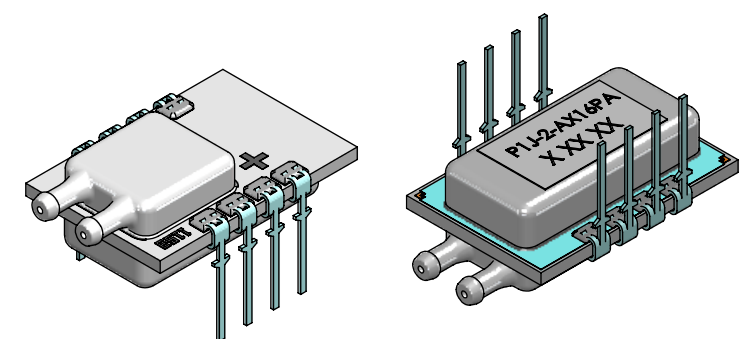
10 10th DAY OF THE MONTH _____

15 CURRENT YEAR _____

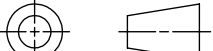





RECOMMENDED PCB LAYOUT

**PROPOSED SPECIFICATIONS
& CONFIGURATIONS FOR
PROTOTYPE ONLY
-SUBJECT TO CHANGE-**



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REMOVE BURRS AND BREAK SHARP EDGES:		DO NOT SCALE THIS DRAWING DIMENSIONS ARE IN MILLIMETERS WITH [INCHES] OPTIONAL DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994 TOL: X ± 0.25 [.XXX ± .010] X.X ± 0.8 [.XX ± .03] FRACT ± 1/32 X.XX ± 0.25 [.XXX ± .010] ANG ± 1/2° DRAFT ANGLE 1/2° MAX ✓ FINISH PER ASME B46.1-2009 ALL MACHINED SURFACES THREADS SHALL BE IN ACCORDANCE WITH ASME B1.1-2003 ABBREVIATIONS PER ASME Y1.1-1989		 <p>THIRD ANGLE PROJECTION PART TO BE CLEAN AND OIL FREE</p>					
MACHINED FILLET RADII TO BE		SPECIAL CHARACTERISTICS PER QCP 154		SEE ECO # 10006749 FOR DOCUMENT APPROVALS ECO DATE: 7/2/19		TITLE <h1>PRESSURE TRANSDUCER</h1>			
	SIGNIFICANT TOTAL NUMBER			CUSTOMER		SIZE B	CODE IDENT NO. 22863	DRAWING NO. P1J rev E-DWG	REV E
	CRITICAL TOTAL NUMBER			CUSTOMER SPEC. NO.					
< S >	SAFETY CRITICAL TOTAL NUMBER			CUSTOMER DWG. NO.		SCALE NONE	CAD: SOLIDWORKS	SHEET 1 OF 3	
UNLESS OTHERWISE SPECIFIED									

I²C COMMUNICATION

I²C INTERFACE:

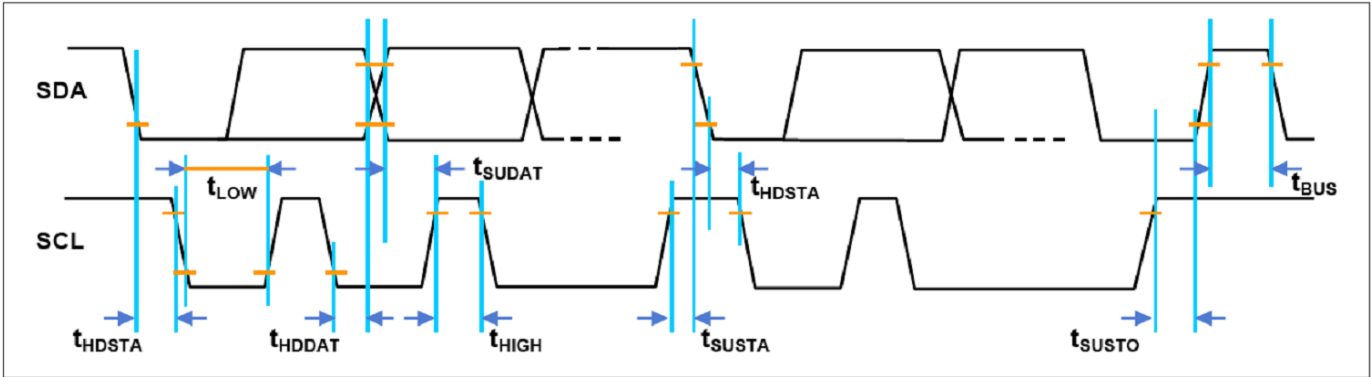
OUTPUT						
RESOLUTION	12 Bits MINIMUM (11 BITS MINIMUM FOR 0-2" AND 0-5mb RANGE)					
UPDATE RATE	0.5 ms					
VOLTAGE	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HIGH-LEVEL INPUT VOLTAGE	V _{IH}	-	0.8 X V _{DD}	-	V _{DD}	V
LOW-LEVEL INPUT VOLTAGE	V _{IL}	-	-	-	0.2 X V _{DD}	V
HIGH-LEVEL OUTPUT VOLTAGE	V _{OH}	-	V _{DD} -0.2	-	V _{DD}	V
LOW-LEVEL OUTPUT VOLTAGE	V _{OL}	-	0	-	0.2	V
PARAMETER						
OUTPUT SOURCING CURRENT	I _{OH_SDA}	SDA @V _{OH} , MIN	-1.9	-3.1	-4.8	mA
	I _{OH_INT}	INT @V _{OH} , MIN	-0.63	-1.2	-1.9	mA
OUTPUT SINK CURRENT	I _{OL_SDA}	SDA @V _{OL} , MAX	2.3	3.9	6.2	mA
	I _{OL_INT}	INT @V _{OL} , MAX	0.85	1.7	3.0	mA
LOAD CAPACITANCE AT SDA	C _{SDA}	@ 400kHz	-	-	200	pF
PULL-UP RESISTOR	R _{I2C_PU}	-	0.5	1	50	kΩ
INPUT CAPACITANCE (EACH PIN)	C _{I2C_IN}	-	-	-	10	pF

TIMING:

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SCL clock frequency	f _{SCL}	100		400	kHz
Start condition hold time relative to SCL edge	t _{HDSTA}	0.1			μs
Minimum SCL clock low width ¹⁾	t _{LOW}	0.6			μs
Minimum SCL clock high width ¹⁾	t _{HIGH}	0.6			μs
Start condition setup time relative to SCL edge	t _{SUSTA}	0.1			μs
Data hold time on SDA relative to SCL edge	t _{HDDAT}	0			μs
Data setup time on SDA relative to SCL edge	t _{SUDAT}	0.1			μs
Stop condition setup time on SCL	t _{SUSTO}	0.1			μs
Bus free time between stop condition and start condition	t _{BUS}	2			μs

1) Combined low and high widths must equal or exceed minimum SCLK period.

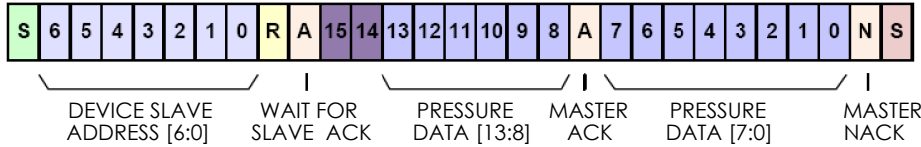
TIMING DIAGRAM:



NOTE: THERE ARE THREE ADJUSTMENTS TO THE I²C IMPLEMENTATION COMPARED WITH THE ORIGINAL I²C PROTOCOL:

- Sending a start-stop condition without any transitions on the CLK line (no clock pulses in between) creates a communication error for the next communication, even if the next start condition is correct and the clock pulse is applied. An additional start condition must be sent, which results in restoration of proper communication.
- The restart condition—a falling SDA edge during data transmission when the CLK clock line is still high—creates the same situation. The next communication fails, and an additional start condition must be sent for correct communication.
- A falling SDA edge is not allowed between the start condition and the first rising SCL edge. If using an I²C™ address with the first bit 0, SDA must be held low from the start condition through the first bit.

I²C COMMUNICATION:



DIAGNOSTIC FEATURES:

THE P1J OFFERS A FULL SUITE OF DIAGNOSTIC FEATURES TO ENSURE ROBUST SYSTEM OPERATION. THE DIAGNOSTIC STATES ARE INDICATED BY A TRANSMISSION OF THE STATUS OF THE 2 MSBs OF THE BRIDGE HIGH BYTE DATA OR BY A SATURATED OUTPUT AT 3FFF_H

STATUS BITS (2 MSBs OF OUTPUT PACKAGE)	DEFINITION
00	NORMAL OPERATION, GOOD DATA PACKET
01	RESERVED (WILL NOT BE SEEN DURING OPERATION)
10	STALE DATA: DATA THAT HAS ALREADY BEEN FETCHED SINCE THE LAST MEASUREMENT CYCLE. NOTE: IF A DATA FETCH IS PERFORMED BEFORE OR DURING THE FIRST MEASUREMENT AFTER POWER-ON RESET, THEN "STALE" WILL BE RETURNED, BUT THIS DATA IS ACTUALLY INVALID BECAUSE THE FIRST MEASUREMENT HAS NOT BEEN COMPLETED
11	DIAGNOSTIC CONDITION EXISTS

- S Start Condition
- 5 Device Slave Address (example: Bit 5)
- 2 Data Bit (example: Bit 2)
- R Read/Write Bit (example: Read=1)
- A Acknowledge (ACK)
- N No Acknowledge (NACK)
- S Stop Condition
- Status Bit

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SPI COMMUNICATION

SPI READINGS WILL BE PROVIDED IN A DUPLEX 3-WIRE READ ONLY FORMAT. THE ENTIRE OUTPUT PACKET CONSISTS OF 4 BYTES (32 bits). THE HIGH BYTE OF THE PRESSURE DATA IS TRANSMITTED FIRST, FOLLOWED BY THE LOW BYTE. THEN 14 bits OF OPTIONAL TEMPERATURE DATA [(TC 13:0)] ARE SENT. THE LAST 2 bits OF THE FINAL BYTE ARE "DO NOT CARE" AND SHOULD BE IGNORED. IF THE OPTIONAL TEMPERATURE DATA IS REQUIRED, PLEASE CONTACT THE KAVLICO SALES TEAM. FOR ALL OTHER APPLICATIONS, THE READ CAN BE TERMINATED AFTER THE 2ND BYTE.

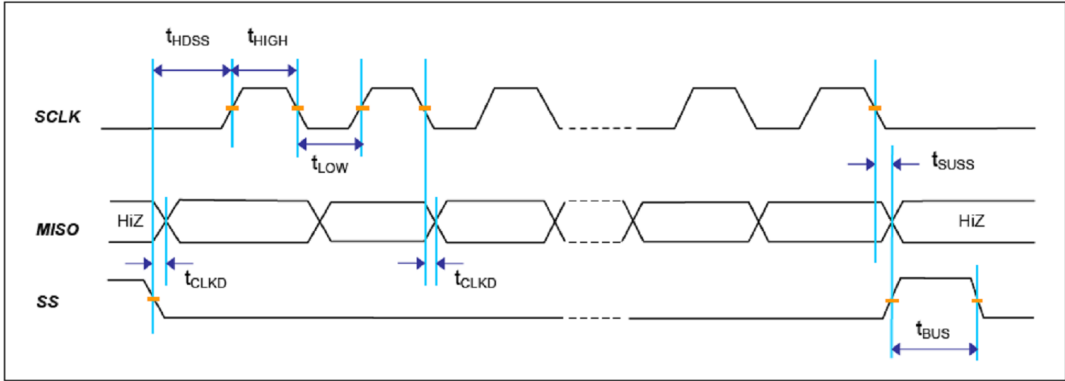
SPI INTERFACE:

OUTPUT						
RESOLUTION	12 Bits MINIMUM (11 BITS MINIMUM FOR 0-2" AND 0-5mb RANGE)					
UPDATE RATE	0.5 ms					
VOLTAGE	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HIGH-LEVEL INPUT VOLTAGE	V _{IH}	-	0.8 X V _{DD}	-	V _{DD}	V
LOW-LEVEL INPUT VOLTAGE	V _{IL}	-	-	-	0.2 X V _{DD}	V
HIGH-LEVEL OUTPUT VOLTAGE	V _{OH}	-	V _{DD} -0.2	-	V _{DD}	V
LOW-LEVEL OUTPUT VOLTAGE	V _{OL}	-	0	-	0.2	V
PARAMETER						
OUTPUT SOURCING CURRENT	I _{OH_MISO}	MISO @V _{OH} , MIN	-1.9	-3.1	-4.8	mA
	I _{OH_SS}	SS @V _{OH} , MIN	-0.63	-1.2	-1.9	mA
OUTPUT SINK CURRENT	I _{OL_MISO}	MISO @V _{OL} , MAX	2.3	3.9	6.2	mA
	I _{OL_SS}	SS @V _{OL} , MAX	0.85	1.7	3.0	mA
INPUT CAPACITANCE (EACH PIN)	C _{I2C_IN}	-	-	-	10	pF

TIMING:

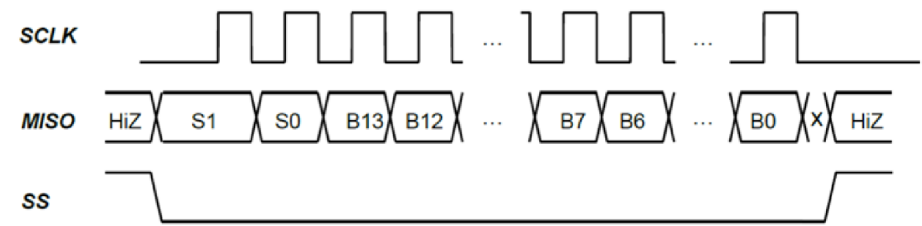
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SCLK clock frequency	f _{SCL}	50		800	kHz
SS drop to first clock edge	t _{HDSS}	2.5			μs
Minimum SCLK clock low width ¹⁾	t _{LOW}	0.6			μs
Minimum SCLK clock high width ¹⁾	t _{HIGH}	0.6			μs
Clock edge to data transition	t _{CLKD}	0		0.5	μs
Rise of SS relative to last clock edge	t _{SUSS}	0.1			μs
Bus free time between rise and fall of SS	t _{BUS}	2			μs
1) Combined low and high widths must equal or exceed minimum SCLK period.					

TIMING DIAGRAM:



NOTE: THE MISO LINE IS SETUP TO CHANGE STATE ON THE FALLING EDGE OF THE SCLK CLOCK. ACCORDINGLY, THE MASTER SHOULD SAMPLE THE DATA ON THE RISING EDGE OF THE SCLK SIGNAL.

OUTPUT PACKET WITH POSITIVE EDGE SAMPLING:



PACKET = [{S(1:0)}, B(13:8)}, { B(7:0)}] WHERE
S(1:0) = STATUS bits OF PACKET (NORMAL, STALE DIAGNOSTIC)
B(13:8) = UPPER 6 bits OF 14-bit PRESSURE DATA
B(7:0) = LOWER 8 bits OF 14-bit PRESSURE DATA
HiZ = HIGH IMPEDANCE

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11	DIAGNOSTIC CONDITION EXISTS

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